In the Claims:

1. (Currently Amended) A nonvolatile memory element having a changeover material ~~(2)~~ and two electrically conductive electrodes ~~(1, 3)~~ present at the changeover material ~~(2)~~ and serving for the application of a voltage and generation of an electric field ~~(E)~~ in the changeover material ~~(2)~~, ~~after a forming step~~ at least two different conductivity states ~~(ON, OFF)~~ prevailing in the changeover material ~~(2)~~, between which changeover can be repeatedly effected by the application of predetermined programming voltages ~~(V_{write}, V_{erase})~~,

wherein at least one of the electrodes ~~(1, 3)~~ has at least one field amplifier structure ~~(4)~~ for amplifying a field strength of the electric field ~~(E)~~ in the changeover material ~~(2)~~.

2. (Currently Amended) The nonvolatile memory element as claimed in ~~patent~~ claim 1, wherein the field amplifier structure constitutes a projection of the electrodes ~~(1, 3)~~ which projects into the changeover material ~~(2)~~.

3. (Currently Amended) The nonvolatile memory element as claimed in ~~patent~~ claim 2, wherein the projection constitutes a tip, corner or edge of the electrodes ~~(1, 3)~~.

4. (Currently Amended) The nonvolatile memory element as claimed in ~~patent~~ claim 3, wherein an angle of the tip, corner or edge is ≤ 90 degrees.

5. (Currently Amended) The nonvolatile memory element as claimed in ~~one of patent~~ claims ~~1 to 4~~, wherein the changeover material ~~(2)~~ has a hydrogen-saturated amorphous semiconductor material.

6. (Currently Amended) The nonvolatile memory element as claimed in ~~one of patent~~ claims ~~1 to 5~~, wherein the changeover material ~~(2)~~ has a multilayer construction ~~(2A, 2B, 2C)~~.

7. (Currently Amended) The nonvolatile memory element as claimed in ~~one of patent~~ claims ~~1 to 5~~, wherein the electrodes ~~(1, 3)~~ have a metal.

8. (Currently Amended) A method for producing a nonvolatile memory element having the following steps:

a) preparation of a carrier material ~~(T)~~;

b) formation of an auxiliary layer ~~(I)~~;

c) formation of a depression ~~(V)~~ in the auxiliary layer ~~(I)~~;

d) filling of the depression ~~(V)~~ with a first electrically conductive material for forming a first electrode ~~(1)~~;

e) formation of at least one field amplifier structure ~~(4A)~~ at the first electrode ~~(1)~~;

f) formation of a changeover material ~~(2)~~ on the first electrode ~~(1)~~ with the field amplifier structure ~~(4A)~~, after ~~a forming step~~which at least two different conductivity states ~~(ON, OFF)~~ prevailing in the changeover material ~~(2)~~, between which changeover can be repeatedly effected by the application of predetermined programming voltages ~~(V_{write}, V_{erase})~~; and

g) formation of a second electrically conductive electrode ~~(3)~~ on the changeover material ~~(2)~~.

9. (Currently Amended) The method as claimed in ~~patent~~ claim 8, wherein, in step a), a semiconductor substrate is prepared as the carrier material ~~(T)~~.

10. (Currently Amended) The method as claimed in ~~patent~~ claim 8 ~~or 9~~, wherein, in step a), a word line ~~(WL)~~ is formed in the carrier material ~~(T)~~ in ~~the~~ a region of the depression ~~(V)~~, the word line ~~(WL)~~ having a material which realizes an ohmic or diode junction ~~(DI)~~ with the material of the first electrode ~~(1)~~.

11. (Currently Amended) The method as claimed in ~~patent~~ claim 8 ~~or 9~~, wherein, in step a), a selection transistor ~~(AT)~~ having source/drain regions ~~(S/D)~~ is formed in the carrier material ~~(T)~~, the source/drain regions

~~(S/D)~~ in each case realizing a bit line ~~(BL)~~ and a terminal region for the first electrode ~~(1)~~.

12. (Currently Amended) The method as claimed in ~~one of patent~~ claim~~s~~ ~~8 to 11~~, wherein, in step b), an insulator layer ~~(I)~~ is deposited over the whole area on the carrier material ~~(T)~~.

13. (Currently Amended) The method as claimed in ~~one of patent~~ claim~~s~~ ~~8 to 12~~,

wherein, in step c),

a resist layer is formed and patterned;

at least part of the auxiliary layer ~~(I)~~ is removed using the patterned resist layer;

the resist layer is removed; and

~~a~~ cleaning ~~step~~ is carried out.

14. (Currently Amended) The method as claimed in ~~patent~~ claim 13, wherein, in step c), ~~an~~ anisotropic etching is carried out for the at least partial removal of the auxiliary layer ~~(I)~~.

15. (Currently Amended) The method as claimed in ~~one of patent~~ claim~~s~~ ~~8 to 14~~, wherein, in step c), a trench or a hole is formed as the depression ~~(V)~~.

16. (Currently Amended) The method as claimed in ~~one of patent~~ claim~~s~~ ~~8 to 15~~, wherein, in step d), the electrically conductive material ~~(1)~~ is deposited in such a way that an adapted depression ~~(VV)~~ is produced in ~~the~~ a region of the depression ~~(V)~~.

17. (Currently Amended) The method as claimed in patent claim 16,

wherein,

in step e),

e11) the electrically conductive material ~~(1)~~ is etched back conformally at least as far as ~~the~~ a surface of the auxiliary layer ~~(I)~~ by ~~means of an~~ anisotropic etching ~~method~~; and

e12) the auxiliary layer ~~(I)~~ is etched back essentially as far as ~~the~~ a bottom region of the adapted depression ~~(VV)~~ by ~~means of an~~ anisotropic etching ~~method~~.

18. (Currently Amended) The method as claimed in ~~one of patent~~ claims ~~8 to 16~~,

wherein,

in step e),

e21) the electrically conductive material ~~(1)~~ is caused to recede at least as far as ~~the~~ a surface of the auxiliary layer ~~(I)~~ by ~~means of a~~ planarization ~~method~~; and

e22) the auxiliary layer ~~(I)~~ is etched back by a predetermined amount ~~(d1)~~ by ~~means of a~~ selective etching ~~method~~.

19. (Currently Amended) The method as claimed in ~~one of patent~~ claims ~~8 to 16~~,

wherein,

in step e),

e31) at least a predetermined amount ~~(d2)~~ of the electrically conductive material ~~(1)~~ is removed in the depression ~~(V)~~ by ~~means of an~~ etching ~~method~~;

e32) ~~a formation of~~ forming a thin conformal electrically conductive layer is carried out in such a way that an adapted depression ~~(VV)~~ remains in ~~the~~ a region of the depression ~~(V)~~;

e33) the electrically conductive layer ~~(1)~~ is etched back at least as far as ~~the~~ a surface of the auxiliary layer ~~(I)~~ by ~~means of an~~ anisotropic etching ~~method~~; and

e34) the auxiliary layer ~~(I)~~ is etched back essentially as far as ~~the~~ a bottom region of the adapted depression ~~(VV)~~ by ~~means of an~~ anisotropic etching ~~method~~.

20. (Currently Amended) The method as claimed in ~~one of patent~~ claims ~~8 to 19~~, wherein, in step f), a single or multiple hydrogen-saturated, amorphous semiconductor layer is deposited on the first electrode ~~(1)~~ with the field amplifier structure ~~(4; 4A, 4B)~~.

21. (Currently Amended) The method as claimed in ~~one of patent~~ claims ~~8 to 20~~, wherein, in step g), a Cr, Au, Al, Cu, NiCr, Ag, Ni, Mo, V, Co, Fe, W or Mn layer is deposited as the second electrode ~~(3)~~.

22. (Currently Amended) A memory element arrangement having a multiplicity of nonvolatile memory elements as claimed in ~~one of patent~~ claims ~~1 to 7~~ which are arranged in matrix form and can be addressed via bit lines ~~(BL)~~ arranged in column form and word lines ~~(WL)~~ arranged in row form,

wherein a respective first electrode ~~(1)~~ is electrically connected via a diode junction ~~(DI)~~ to a respective word line ~~(WL)~~ formed in a semiconductor substrate ~~(T)~~, and

a respective second electrode ~~(3)~~ for forming a respective bit line ~~(BL)~~ is patterned in strip form at ~~the~~ a surface of ~~the~~ an auxiliary layer ~~(I)~~.

23. (Currently Amended) A memory element arrangement having a multiplicity of nonvolatile memory elements as claimed in ~~one of patent~~ claims ~~1 to 7~~ which are arranged in matrix form and can be addressed via bit lines ~~(BL)~~ arranged in column form and word lines ~~(WL)~~ arranged in row form,

wherein a respective first electrode ~~(1)~~ is electrically connected via an ohmic junction to a respective word line ~~(WL)~~ formed in a semiconductor substrate ~~(T)~~, and

a respective second electrode ~~(3)~~ for forming the respective bit line ~~(BL)~~ is patterned in strip form at the surface of ~~the~~ an auxiliary layer ~~(I)~~.

24. (Currently Amended) A memory element arrangement having a multiplicity of nonvolatile memory elements as claimed in ~~one of patent~~ claims ~~1 to 7~~ which are arranged in matrix form and can be addressed via bit lines ~~(BL)~~ arranged in column form and word lines ~~(WL)~~ arranged in row form,

wherein there is formed, for each memory element ~~(SE)~~, a selection transistor ~~(AT)~~ with a word line ~~(WL)~~ serving as control layer and a bit line ~~(BL)~~ serving as first source/drain region ~~(S/D)~~ in the semiconductor substrate ~~(T)~~, a second source/drain region ~~(S/D)~~ of the selection transistor ~~(AT)~~ being electrically connected to a first electrode ~~(1)~~ of the memory element ~~(SE)~~ and a respective second electrode ~~(3)~~ being at a common potential.